CLAIMS

What is claimed is:

1.   1. A method comprising:

2.   using processor implementation-specific instructions to save a

3.   processor state in a system memory when a machine check

4.   error is generated by a processor;

5.   attempting to correct the error using processor implementation-

6.   specific instructions;

7.   transferring control to processor-independent instructions;

8.   receiving control from processor-independent instructions; and

9.   returning to an interrupted context of the processor by restoring

10.   the processor state.

1.   2. The method of claim 1, further comprising providing processor

2.   error record information obtained using processor implementation-

3.   specific instructions.

1.   3. The method of claim 1, further comprising attempting to contain

2.   the error if a second processor is coupled to the processor by

3.   requesting a rendezvous between the processor and the second

4.   processor.

1.   4. The method of claim 1, wherein receiving control from processor-

2.   independent instructions indicates that the error has been
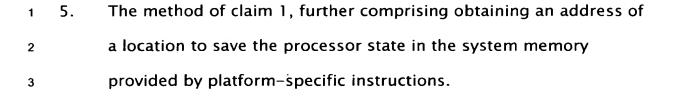
3.   corrected.

1   5.   The method of claim 1, further comprising obtaining an address of

2   a location to save the processor state in the system memory

3   provided by platform-specific instructions.

1   6.   The method of claim 1, wherein attempting to correct the error

2   using processor implementation-specific instructions is not done if

3   an expected machine check indicator is set.

1   7.   A machine-readable medium that provides instructions that, if

2   executed by a processor, will cause the processor to perform

3   operations comprising:

4   using processor implementation-specific instructions to save the

5   processor state in a system memory when a machine check

6   error is generated by the processor;

7   attempting to correct the error using processor implementation-

8   specific instructions;

9   transferring control to processor-independent instructions;

10   receiving control from processor-independent instructions; and

11   returning to an interrupted context of the processor by restoring

12   the processor state.

1   8.   The machine-readable medium of claim 7, wherein the operations

2   further comprise using processor implementation-specific

3   instructions to provide processor error record information

4   requested by processor-independent instructions.

1   9.   The machine-readable medium of claim 7, wherein the operations

2   further comprise attempting to contain the error if a second

3   processor is coupled to the processor by requesting a rendezvous

4   between the processor and the second processor.

1   10.   The machine-readable medium of claim 7, wherein receiving

2   control from processor-independent instructions indicates that the

3   error has been corrected.

1   11.   The machine-readable medium of claim 7, wherein the operations

2   further comprise obtaining an address of a location to save the

3   processor state in the system memory provided by platform-

4   specific instructions.

1   12.   The machine-readable medium of claim 7, wherein attempting to

2   correct the error using processor implementation-specific

3   instructions is not done if an expected machine check indicator is

4   set.

1   13.   The machine-readable medium of claim 7, wherein the instructions

2   provided by the machine-readable medium are not cacheable by

3   the processor.

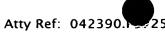1   14.   A central processing unit (CPU) comprising:

2   a processor;

3   a first machine-readable medium coupled to the processor, the

4   first machine-readable medium including processor

5   implementation-specific instructions that, if executed by the

6   processor, will cause the processor to perform operations

7   including

8   saving the processor state in a system memory and

9   attempting to correct the error when a machine check

10   error is generated by the processor, and

11   receiving control and returning to the interrupted context of

12   the processor by restoring the state of the processor

13   when the error is determined to have been corrected;

14   a second machine-readable medium coupled to the processor, the

15   second machine-readable medium including only processor

16   implementation-independent instructions that, if executed by

17   the processor, will cause the processor to perform operations

18   including

19   receiving control from the first machine-readable medium;

20   determining if the error has been corrected;

21   transferring control to the first machine-readable medium if

22   the error has been corrected.

1   15.   The central processing unit (CPU) of claim 14, wherein the
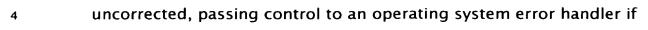
2   operations performed by the instructions provided by the second

3   machine-readable medium further include requesting processor

4   error record information from the first machine-readable medium.

1   16.   The central processing unit (CPU) of claim 14, wherein the

2   operations performed by the instructions provided by the first

3   machine-readable medium further include attempting to contain

4   the error if a second processor is coupled to the processor by

5   requesting a rendezvous between the processor and the second

6   processor.

1   17.   The central processing unit (CPU) of claim 14, wherein the

2   operations performed by the instructions provided by the second

3   machine-readable medium further include providing an address of

4   a location to save the processor state in the system memory to the

5   first machine-readable medium.

1   18.   The central processing unit (CPU) of claim 14, wherein attempting

2   to correct the error is not done if an expected machine check

3   indicator is set.

1   19.   The central processing unit (CPU) of claim 14, wherein the

2   instructions provided by the first and second machine-readable

3   media are not cacheable by the processor.

1   20.   The central processing unit (CPU) of claim 14, wherein the

2   operations performed by the instructions provided by the second

3   machine-readable medium further include if the error is

4   uncorrected, passing control to an operating system error handler if

5   present, otherwise, performing one of a halt and a reboot of the

6   CPU.